ABSTRACT

A timing of a receiving slot at the wireless receiving section 11 is detected at the interrupt generation section 12, which generates a receiving slot start interrupt signal (b) and a receiving slot end interrupt signal (c), during a period between a relevant receiving slot start interrupt signal (a) and a receiving slot end interrupt signal (c), an operation clock frequency of the CPU 21 in the data processing section 2 is variably controlled according to a receiving electric field strength, whereby the deterioration of receiving performance due to noises running from the data processing section 2 to the wireless section 1 at the receiving time can be reduced.